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Abstract
Since the critical dimension (CD) in the nano-scaled fabrication is way smaller than the wavelength, diffraction might create serious problem such as optical proximity effect (OPE) and cause distortion of the masked prints. Furthermore, other types of distortion might include errors in the wire length when we perform lithography on the wafer, which might cause the yield to go down in the production.
This thesis offers a method of automation in circuit layout by using dynamic programmable logic array (DPLA), which reduces the cost of performing the optical proximity correction (OPC). In the average DPLA circuit design, engineers intend to design the circuit with emphasis on the circuit performance but without the circuit yields. Also, when the OPC is performed, most of the fabrication manufacturers do run an overall correction, which is time-consuming and high cost. We intend to use the proposed algorithm to pre-arrange the product lines in the DPLA without affecting the functionality and the increase of the area by reducing the adjacent transistors that couple together with the possible minimization of the interference between two prints in terms of design costs. According to the experiment we have done on 28 different circuits, we have obtained a drastic improvement to nearly 31% of the original OPC cost. Moreover, we use the DPLA compiler and automatically generate DPLA configuration and the corresponding critical path with the help of the optical simulation software SPLAT for a more reliable distortion analysis. Finally, the analysis on comparing the performance of circuits could be the reference for the OPC.
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